

ULTRA SMALL SIZE VERTICAL MOSFET DEVICE AND
METHOD FOR THE MANUFACTURE THEREOF

Field of the Invention

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The present invention relates to a MOSFET (metal oxide semiconductor field effect transistor) device; and, more particularly, to an ultra small size vertical MOSFET device having a vertical channel and a source/drain structure and a 10 method for the manufacture thereof by using a silicon on insulator (SOI) substrate.

Description of the Prior Art

15 In a silicon device technology, it is necessary to reduce a length of a channel, a depth of metallurgical junction at source and drain contact and a thickness of an effective gate insulating layer for achieving the silicon device with a low voltage, a high integration and a high speed drivability. 20 Additionally, it is required the device with a high performance characteristic by an increase of a driving current and a decrease of a leakage current among the same size of the devices.

However, it has lot of obstacles to manufacture a nano-25 scale silicon device with a high performance by using a conventional manufacturing method. That is, in case of manufacturing a planar channel of a nano-scale by the

conventional method, a special patterning method such as an e-beam direct writing method or x-ray lithography method should be used. But it is impossible to manufacture the nano-scale silicon device in large quantities because the e-beam direct 5 writing method and x-ray lithography method are not definite techniques up to now. Furthermore, since it is not only difficult to fabricate the nano-scale device with shallow source/drain junction depth using a single crystal silicon material but an electrical isolation property may also be 10 deteriorated, there are difficulties in fabricating the device with the low voltage drivability. Thus, in order to overcome the above problems, very complicated manufacturing processes are required.

One conventional method for manufacturing a vertical MOS 15 transistor is disclosed by Mitsui in U.S.Pat. 5,382,816, "Semiconductor Device Having Vertical Transistor with Tubular Double Gate". In accordance with this method, a first gate and a second gate are formed the interior and the exterior of the vertical channel. Thus, a threshold voltage may be 20 controlled by applying voltage to each gate. However, this method has drawbacks that a structure of the MOS transistor is too complicated and further, a plurality of lithography, deposition and etch processes are required. Additionally, it is hard to downsize the device because it is difficult to 25 secure a process margin.

Another conventional method for manufacturing a vertical MOS transistor is disclosed by Kenney in U.S.Pat. 5,365,097,

"Vertical Epitaxial SOI transistor, Memory Cell and Fabrication Methods". In a disclosure, a trench is formed on an SOI substrate and a silicon epi layer is deposited in the trench. Therefore, a memory cell and the MOS transistor 5 fabricated integrally. However, the MOS transistor having the vertical silicon channel in accordance with this conventional method has disadvantages as follows: first, it is difficult to secure a process margin owing to a complicated structure of the device; second, it is hard to fabricate the device in the 10 trench of a micro size; third, it is difficult to grow up a single crystal silicon epi layer on a poly-crystal silicon; fourth, it is difficult to form a p-n junction on the channel of the single crystal and a diffusion layer of the poly-crystal; fifth, since source/drain contacts are formed on the 15 channel of the single crystal and a diffusion layer of the poly-crystal, the junction leakage of source/drain contacts increases, besides a reliability and an insulating property of a gate insulating layer may be deteriorated.

The other conventional method for manufacturing a 20 vertical MOS transistor is disclosed by J.M. Hergenrother in an article, "The Vertical Replacement-Gate MOSFET, IEDM 99, pp.75-78, Dec. 1, 1999". In the article, the method comprises the steps of forming a trench using a single crystal silicon substrate, forming a vertical channel by growing up the single 25 crystal silicon epitaxially, forming a gate enclosing the channel, and forming a source/drain over and below the gate. According to this method, in order to fabricate the MOS

transistor having the vertical silicon channel, complicated manufacturing steps should be carried out. Namely, a trench is formed interior of an insulating layer, first of all. Thereafter, the single crystal silicon epi layer is formed in 5 the trench. Finally, the source/drain is formed. Therefore, it has problems that the manufacturing processes are too complicated and further, it is difficult to interconnect among the unit devices.

As described above, in accordance with the conventional methods, an isolation step is required due to a use of the bulk silicon. Moreover, stringent manufacturing conditions are needed in order to reduce the length of the channel. That is, because it is impossible to form the channel of the nanometer size horizontally by using a conventional 15 photolithography, the e-beam direct writing method or x-ray lithography method should be employed. Although the e-beam direct writing method or x-ray lithography method is used, it is difficult to manufacture the device of nano-meter size in large quantities. The lithography technique is not established 20 in order to manufacture the device of the nanometer size still now. In addition, the conventional method using the silicon single crystal has large problems for forming shallow source/drain junction, ensuring a reliability of the nanometer scale device and isolation of each device electrically.

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Summary of the Invention

It is, therefore, an object of the present invention to provide an ultra small size vertical MOSFET (metal oxide semiconductor field effect transistor) device having a vertical channel and a source/drain structure by applying a 5 diffusion process without additional lithography steps.

It is another object of the present invention to provide a method for manufacturing an ultra small size vertical MOSFET device having high drive current by increasing the channel width in the same chip area.

10 In accordance with one aspect of the present invention, there is provided the ultra small size vertical MOSFET device, comprising: a silicon on insulator (SOI) substrate including a single crystal substrate, an oxide layer formed upon the single crystal substrate and a first single crystal silicon 15 layer formed upon the oxide layer; a first silicon conductive layer formed by doping an impurity of a high concentration into the first single crystal silicon layer; a source contact, a channel and a drain contact formed on the first silicon conductive layer; a gate insulating layer formed on the first silicon conductive layer, the source/drain contacts and the 20 channel; a second silicon conductive layer formed on the drain contact; and a gate electrode formed on side walls of the channel.

In accordance with another aspect of the present 25 invention, there is provided a method for manufacturing an ultra small size vertical MOSFET device, the method comprising the steps of: a) preparing an SOI substrate including a single

crystal substrate, an oxide layer formed upon the single crystal substrate and a first single crystal silicon layer formed upon the oxide layer; b) forming a first silicon conductive layer by doping an impurity of a high concentration 5 into the first single crystal silicon layer; c) forming a second single crystal silicon layer and a second silicon conductive layer on the first silicon conductive layer, wherein the second single crystal silicon layer has the impurity of a low concentration and the second silicon 10 conductive layer has the impurity of a high concentration; d) patterning the second silicon conductive layer and the second single crystal silicon layer vertically into a first predetermined configuration; e) forming a gate insulating layer on the first silicon conductive layer, the second single 15 crystal silicon layer and the second silicon conductive layer; f) carrying out an annealing process to diffuse the impurities in the first silicon conductive layer and the second silicon conductive layer into the second single crystal layer, thereby forming a source contact, a drain contact and a vertical 20 channel; and g) forming a gate electrode on side walls of the vertical channel, wherein the gate electrode encompasses the channel.

Brief Description of the Drawings

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The above and other objects and features of the present invention will become apparent from the following description

of the preferred embodiment given in conjunction with the accompanying drawings, in which:

Figs. 1 to 11 show cross sectional views setting forth an ultra small size vertical MOSFET (metal oxide semiconductor field effect transistor) device and a method for the manufacture thereof in accordance with the present invention.

Detailed Description of the Preferred Embodiments

10 There are provided in Figs. 1 to 11 cross sectional views setting forth an ultra small size vertical MOSET (metal oxide semiconductor field effect transistor) device and a method for the manufacture thereof in accordance with a preferred embodiment of the present invention. It is noted that the 15 same reference numerals are used throughout multiple figures to designate the same components.

In Fig. 11, there is provided a cross sectional view of the inventive ultra small size vertical MOSFET device comprising an SOI (silicon on insulator) substrate, a channel 20 41, a source contact 80, a drain contact 90, a second silicon conductive layer 50, a gate insulating layer 70, a gate electrode 101, an interlayer dielectric (ILD) layer 130, a source interconnection 140, a drain interconnection 150 and a gate electrode interconnection 160. The SOI substrate 25 includes a single crystal substrate 10, an oxide layer 20 formed upon the single crystal substrate 10 and a first silicon conductive layer 31 formed upon the oxide layer 20.

The first silicon conductive layer 31 is formed by doping an impurity of a high concentration into a single crystal silicon layer using a method such as an ion implantation, plasma doping or some diffusion techniques, wherein the 5 impurity material includes a p-typed material or an n-typed material such as boron (B), phosphorus (P) or the like.

In order to achieve the channel 41, a source contact 80 and a drain contact 90, a second single crystal silicon layer and a second silicon conductive layer 50 are formed on the 10 first silicon conductive layer 31, first of all. Thereafter, the second silicon conductive layer 50 and the second single crystal silicon layer are patterned. At this time, the second single crystal silicon layer is formed by using a method such as a chemical vapor deposition (CVD) or a molecular beam 15 epitaxy (MBE) technique. And the second silicon conductive layer is made of an amorphous silicon or a poly-crystal silicon by the CVD technique.

Then, the gate insulating layer 70 is formed on the patterned layers and the first silicon conductive layer, 20 wherein the gate insulating layer is made of a thermal oxide layer, a nitride layer, a CVD oxide layer and a CVD nitride layer.

Since the second single crystal silicon layer has the impurity of a low concentration and the second silicon 25 conductive layer 50 has the impurity of a high concentration, the impurities existing in the first and the second silicon conductive layers 31, 50 diffuse into the second single

crystal silicon layer by an annealing process, thereby obtaining the source contact 80, the channel 41 and the drain contact 90. It is preferable that the annealing process should be carried out at a temperature ranging from 5 approximately 700 °C to approximately 1,000 °C in an electrical furnace or a rapid thermal annealing (RTA) furnace.

The gate electrode 101 is achieved by forming a third silicon conductive layer and patterning into a predetermined configuration using a dry etch process. Then, an ILD layer 10 130 is formed on entire surfaces and patterned, whereby a source, a drain and a gate electrode contact holes are formed. Thereafter, a metal or a silicon conductive layer is deposited 15 into the contact holes, thereby completing a source interconnection 140, a drain interconnection 160 and a gate electrode interconnection 150.

Figs. 1 to 11 are schematic cross sectional views setting forth the method for manufacture of an ultra small size vertical MOSFET device in accordance with the present invention.

20 Referring to Fig. 1, the manufacturing process begins with the preparation of an SOI substrate in which an oxide layer 20 and a first single crystal silicon layer 30 is formed on a single crystal substrate 10, sequentially.

Thereafter, referring to Fig. 2, the first single 25 crystal silicon layer 30 is doped with an impurity of a high concentration using a method such as an ion implantation or a vapor diffusion technique so that a first silicon conductive

layer 31 is obtained, wherein the impurity material includes a p-typed or an n-typed material such as boron (B), phosphorus (P) or the like.

5 In a next step as illustrated in Fig. 3, a second single crystal silicon layer 40 with the impurity of a low concentration is formed on the first silicon conductive layer 31 by using a method such as a CVD or a MBE technique.

10 In an ensuing step as shown in Fig. 4, a second silicon conductive layer 50 with the impurity of a high concentration is formed on the second single crystal silicon layer 40. Here, the second silicon conductive layer 50 is made of an amorphous silicon or a poly-crystal silicon having the impurity material such as the p-typed or the n-typed material by using the CVD technique.

15 Subsequently, an etch mask 60 is formed on the second silicon conductive layer 50. Then, the second single crystal silicon layer 40 and the second silicon conductive layer 50 are vertically patterned into a first predetermined configuration by using a dry etch process, as shown in Fig. 5. 20 The etch mask 60 includes a photoresist, oxide or nitride layer.

25 Thereafter, as depicted in Fig. 6, a gate insulating layer 70 is formed on the first silicon conductive layer 31, the second single crystal silicon layer 40 and the second silicon conductive layer 50 in an oxygen rich ambient. At this time, the gate insulating layer 70 is formed at a temperature ranging from approximately 700 °C to approximately

1,000 °C in an electrical furnace or a rapid thermal annealing (RTA) furnace. The gate insulating layer 70 may be made of a thermal oxide layer, a nitride layer, a CVD oxide layer or a CVD nitride layer.

5 Then, an annealing process is carried out to diffuse the impurities existing in the first silicon conductive layer 31 and the second silicon conductive layer 50 into the second single crystal layer 40, thereby forming a source contact 80, a drain contact 90 and a channel 41. At this time, a length 10 of the channel can be determined by modulating a diffusion depth of the impurities by means of a condition of a post annealing process. That is, in case of shortening the length of the channel 41 of the transistor, the annealing process should be carried out at a high temperature for a long time so 15 that the diffusion depth increases and the length of channel 41 is shortened. Meanwhile, when the annealing process is carried out at a low temperature for a rapid time, the diffusion depth decreases to lengthen the length of the channel 41.

20 In a next step as shown in Fig. 7, a third silicon conductive layer 100 is formed on top of the gate insulating layer 70. Here, the third silicon conductive layer 50 is also made of an amorphous silicon or a poly-crystal silicon having the impurity such as the p-typed material or the n-typed 25 material by using the CVD technique.

 In an ensuing step, a first ILD layer 110 is deposited on the third silicon conductive layer 100 and patterned into a

second predetermined configuration, as shown in Fig. 8.

In a subsequent step, dry etch process is carried out to form a gate electrode 101 on side walls of the channel by using an etch mask 120 formed upon a portion of the first ILD layer 110. Therefore, the gate electrode 101 encompasses the channel 41 as shown in Fig. 9.

Subsequently, after the etch mask 120 and a remained first ILD layer 110 are removed, a second ILD layer 130 is formed upon entire surfaces including the gate electrode 101, the second silicon conductive layer 50 and the gate oxide layer 70, as shown in Fig. 10.

Finally, a source contact hole, a drain contact hole and a gate electrode contact hole are formed by patterning the second ILD layer 130 into a third predetermined configuration, as shown in Fig. 11. Then, a source interconnection 140, a drain interconnection 150 and a gate electrode interconnection 160 are formed by depositing a metal or a silicon conductive layer into the contact holes.

In comparison with the prior art, the present invention provides the ultra small size channel formed by using the diffusion process instead of a conventional photomask and lithography process. Thus, the channel size can be controlled by means of the condition of the diffusion process. In addition, it is unnecessary to carry out the photomask, the lithography, the ion implantation and the impurity-doping process to form the source/drain structure so that whole the manufacturing processes may be simplified. Since there is not

happened any crystal defect during the ion implantation or the annealing process for activating the impurities, a reliability of the inventive MOSFET device may be enhanced.

Moreover, as the vertical channel is formed in the 5 present invention, a width of an effective channel increases in spite of the same area of a chip on the substrate, whereby a high drivability device can be embodied. As SOI substrate is utilized in the present invention, a leakage current may be reduced without a formation of an isolation region.

10 Although the preferred embodiments of the invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying 15 claims.